BURST EDO DRAM

1 MEG x 16

FEATURES

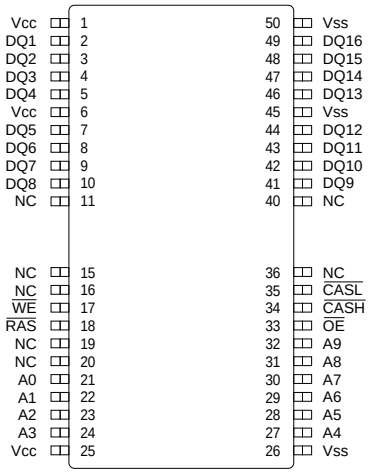
- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- Single power supply: +3.3V ±5%
- All inputs and outputs are LVTTL compatible with 5V input/output tolerance
- Industry-standard x16 pinout and packages
- High-performance CMOS silicon-gate process
- Refresh: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or $\overline{RAS}$ ONLY
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Four-cycle Extended Data-Out (EDO) burst accesses

OPTIONS MARKING

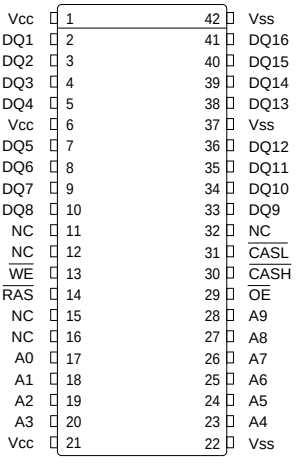
- Timing
  - 52ns access; 15ns cycle -52
  - 60ns access; 16.6ns cycle -60
  - 70ns access; 20ns cycle -70
- Packages
  - Plastic TSOP (400 mil) TG
  - Plastic SOJ (400 mil) DJ
- Refresh
  - Standard (1,024 cycles at 16ms) None
- Part Number Example: MT4LC1M16H5TG-52

PIN ASSIGNMENT (Top View)

44/50-Pin TSOP
(BB-1)



42-Pin SOJ
(BA-3)



GENERAL DESCRIPTION

The MT4LC1M16H5 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at $\overline{RAS}$ time and 10 bits (A0-A9) at $\overline{CAS}$ time.

The MT4LC1M16H5 is a burst access DRAM in which all READ and WORD WRITE access cycles occur in bursts of four. The bursts wrap around on a 4-byte boundry. This means that the two least significant bits of the $\overline{CAS}$ ($\overline{CASL}$ and $\overline{CASH}$) address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with $\overline{WE}$ LOW) with address A0 set to either HIGH or LOW. A0 LOW will program the device to execute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information ($0010\ 000x_B$) where x=A0 is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle to exit this programming mode.

$\overline{RAS}$ HIGH and $\overline{CAS}$ HIGH ($\overline{CASL}$ and $\overline{CASH}$) terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. The chip is precharged for the next access during the $\overline{RAS}$ HIGH time.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (V_{CC} = +3.3V ±5%)

AC CHARACTERISTICS		-52		-60		-70			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from $\overline{CAS}$	^tAA		25		28.2		35	ns	12
Column-address setup time	^tASC	1.5		1.5		1.5		ns	
Row-address setup time	^tASR	1.5		1.5		1.5		ns	
Burst terminate hold time	^tBTH	3		3		3		ns	
Output disable from burst terminate	^tBTHZ	7	13	7	13	7	13	ns	13, 16
Access time from $\overline{CAS}$	^tCAC		10		11		15	ns	
Column-address hold time	^tCAH	8.5		8.5		8.5		ns	
$\overline{CAS}$ pulse width	^tCAS	5	10,000	5	10,000	5	10,000	ns	
$\overline{CASL}$ and $\overline{CASH}$ coincident HIGH time	^tCCH	5		5		5		ns	18
$\overline{CAS}$ hold time (CBR or WCBR)	^tCHR	15		15		15		ns	6
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	13
Data Hold time from $\overline{CAS}$ LOW	^tCOH	3		3		3		ns	
$\overline{CAS}$ precharge time	^tCP	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR or WCBR)	^tCPN	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH (WRITE only)	^tCRW	15		16.6		20		ns	
Skew between $\overline{CASL}$ and $\overline{CASH}$ (WRITE only)	^tCSK		2		2		2	ns	19
$\overline{CAS}$ setup time (CBR or WCBR)	^tCSR	10		10		10		ns	6
Data-in hold time	^tDH	5		5		5		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Ouput Disable	^tOD	4	10	4	10	4	15	ns	13
Ouput Enable access time	^tOEA		10		12		15	ns	
Ouput Enable hold (only near $\overline{CAS}$)	^tOEH	5		5		5		ns	
$\overline{OE}$ to output in Low-Z	^tOELZ	3		3		3		ns	13
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		10		ns	
Ouput Enable setup (only near $\overline{CAS}$)	^tOES	3		3		3		ns	
Output buffer turn-off delay	^tOFF	4	10	4	10	4	15	ns	13
Burst EDO cycle time	^tPC	15		16.6		20			
Access time from $\overline{RAS}$	^tRAC		52		60		70	ns	
Row-address hold time	^tRAH	8.5		8.5		8.5		ns	
$\overline{RAS}$ pulse width	^tRAS	52	125,000	60	125,000	70	125,000	ns	
Random Read or Write cycle time	^tRC	90		110		130			
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD1$	20		20		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD2$	40		45		55		ns	
Read command hold time	^tRCH	5		5		5		ns	
Read command setup time	^tRCS	3		4		5		ns	
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ precharge time	^tRP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	5		5		5		ns	
$\overline{RAS}$ hold time	^tRSH	0		0		0		ns	
Transition time (rise or fall)	^tT	1.5	50	1.5	50	1.5	50	ns	
Burst Terminate pulse width	^tTP	6		6		8		ns	14
Write command hold time	^tWCH	5		5		5		ns	
$\overline{WE}$ command setup time	^tWCS	3		4		5		ns	
Ouput Disable from $\overline{WE}$ LOW	^tWHZ	4	10	4	10	4	15	ns	13, 16
$\overline{WE}$ hold time (CBR or WCBR)	^tWRH	10		10		10		ns	
$\overline{WE}$ setup time (CBR or WCBR)	^tWRP	10		10		10		ns	